Field Emission from Silicon Tips Embedded in a Dielectric Matrix


*Massachusetts Institute of Technology, Cambridge, MA, 02139
**Creative MicroSystems, Waitsfield, VT, 056732
***University of Cambridge, Cambridge, CB30FA, UK
*Corresponding author: karaulac@mit.edu

Field electron emission from conducting surfaces requires high fields and pristine surfaces. These surfaces are vulnerable to adsorption-desorption processes by residual gas molecules leading to emission current fluctuations, tip erosion, etc. However, electron transport through insulators often leads to impact ionization and dielectric breakdown. This abstract explores electron emission from field emitter tips that are embedded in a dielectric matrix, specifically silicon dioxide, as a potential approach to address reliability problems in classical field emitters.

The devices presented in this abstract are arrays of silicon field emitter tips which are individually regulated by silicon nanowires that were previously reported in [1]. The silicon nanowires have diameters between 100-200 nm and heights of 10 µm resulting in an aspect ratio of 50-100:1. The emitter tips have radii of 5 nm with a log-normal distribution (σ = 1.2 nm) and a density of 10^8 tips/cm^2. Further, the silicon nanowires function as current limiters which improve reliability by preventing premature tip burn-out due to Joule heating, thermal runaway, and cathodic arcs. Chemical mechanical polishing (CMP) was used to form the self-aligned gates. The emitter tips were not released in BOE but remained embedded in 50 nm of SiO_2. In addition, a single layer of graphene was deposited on a copper substrate and transferred on top of the polysilicon gates using PMMA [2, 3]. The graphene layer creates an equipotential surface above the tip. A diagram of the final structure is shown in figure 1.

The anode current was measured from different size arrays. Figure 2 shows the data collected from a 1000x1000 emitter array. FN analysis of the data shows that the emitted current is barrier limited. In addition, the common gate current gain (α_F = I_A/I_E) was analyzed. FN analysis of the emitter and anode currents suggests that the effective barriers for the emitter and anode currents have different values. Additional data and analysis shall be provided at the conference.

**Figure 1.** Diagram of a silicon field emitter tip embedded in silicon dioxide with single layer graphene on top.

**Figure 2.** I-V plot showing anode current vs. gate-emitter voltage. FN-plot showing FN slope and FN intercept.

References